Clock Distribution

Roger Cappallo
MIT Haystack Observatory
MWA Seattle Meeting
2009.6.17

Clock Distribution Overview

- System timing currently supplied by an RRI-built module
- Centrally located, external to receivers & connected by coax
- Next generation of “fieldable” receivers requires a distributed clock subsystem, with timing signals carried by optical fibre
- Design work & prototype contracted to Finish Line Product Development Services in Hudson, NH

Clock Distributor

- **Functions**
  - Receive 655.36 MHz from external frequency source (HP8642A driven by Symetricom XL-GPS rcvr.)
  - Modulate this signal with 1 PPS signal (from GPS)
  - Distribute combined signal to 64 receivers through laser drivers
- **Components**
  - 1 Clock Modulator PCB
  - 8 Fibre Optic Driver PCB’s
  - 64 SFP laser transceivers

Clock Distributor (cont'd.)

- **Implementation**
  - Clock Modulator PCB (1X)
  - Fibre Optic Driver PCB (8X)
  - either 64 SFP transceivers or 32 SFP dual Tx's

Clock Modulator - Simplified Block Diagram

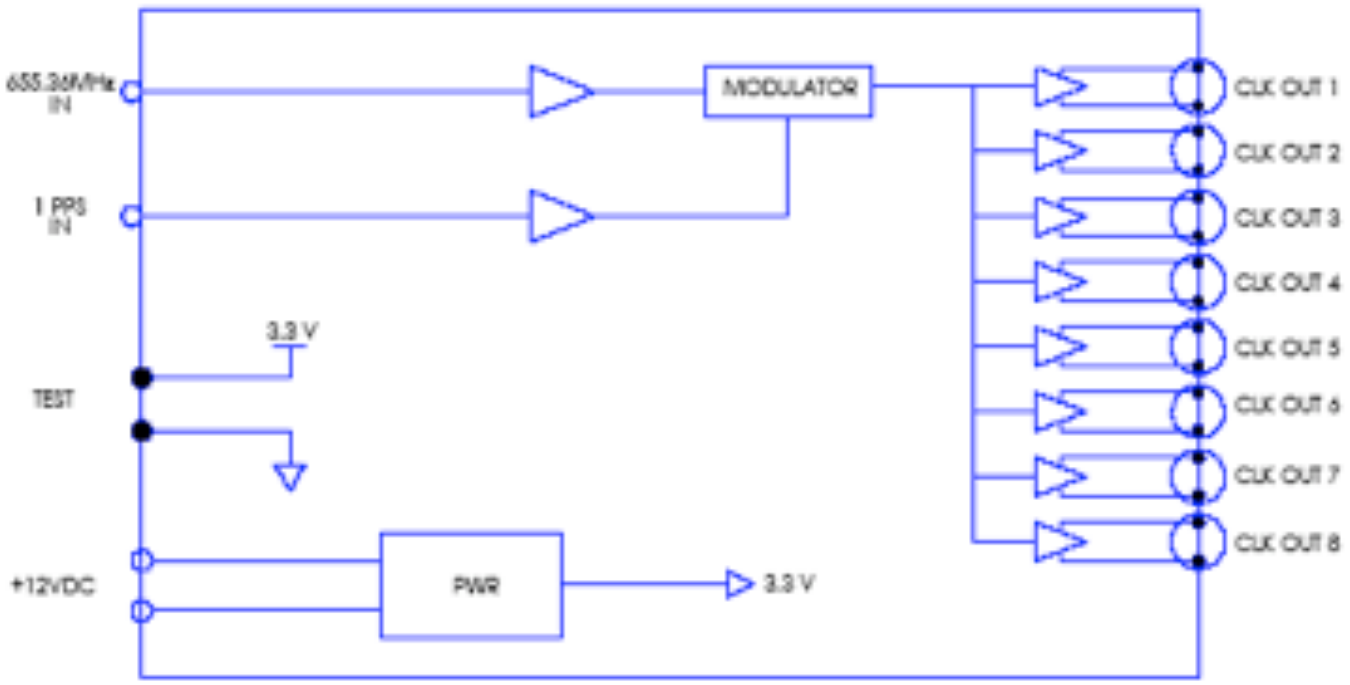


FIGURE 1A - SYSTEM OVERVIEW - CLOCK MODULATOR

Fibre Optic Driver - Simplified Block Diagram

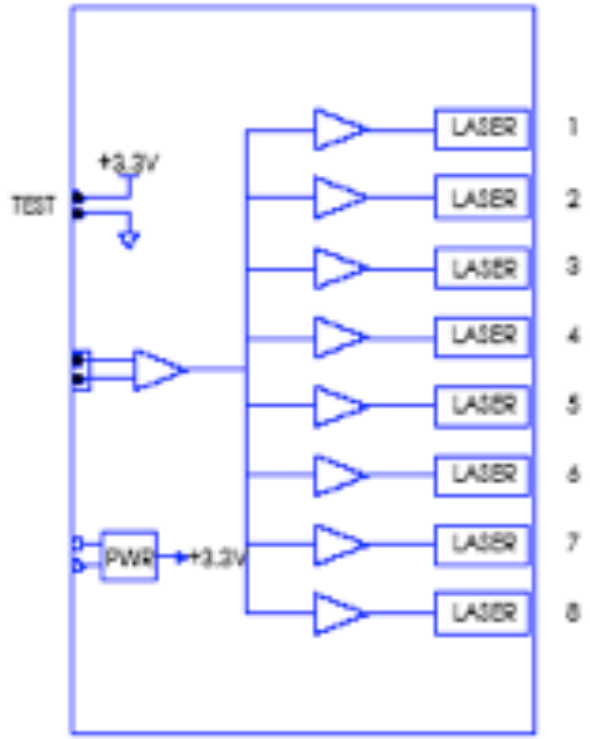
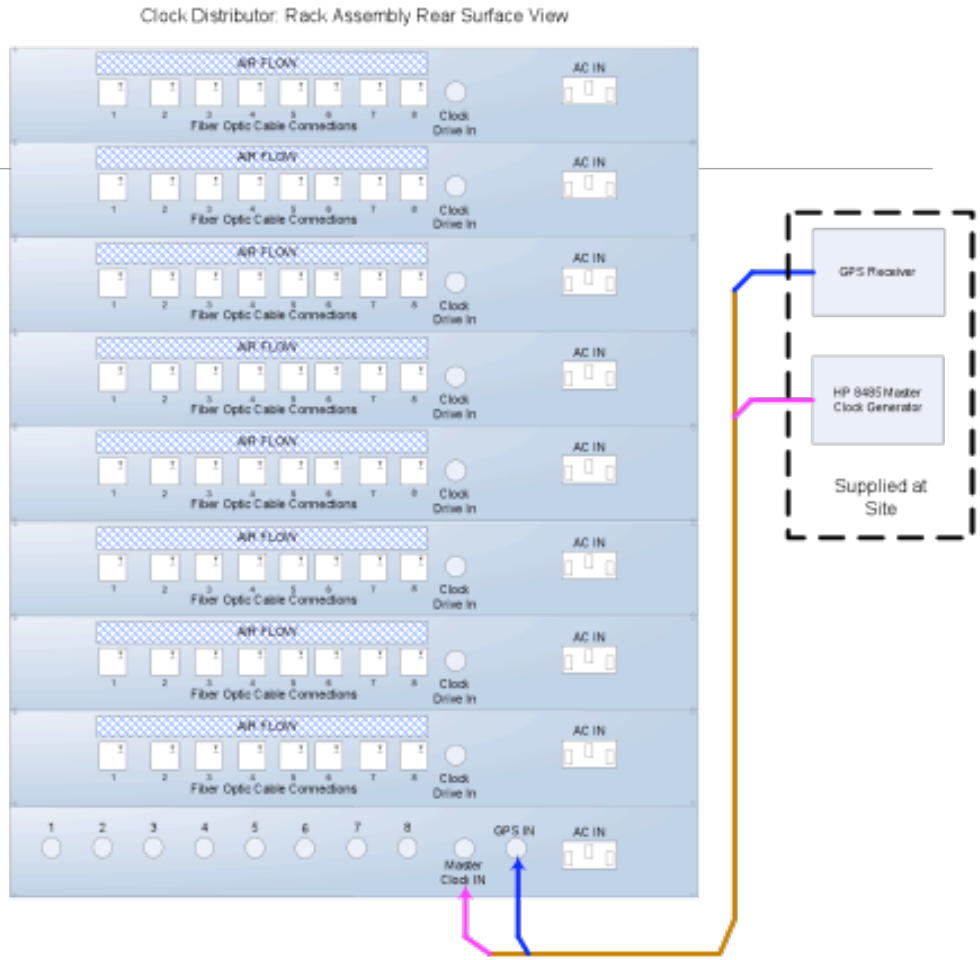
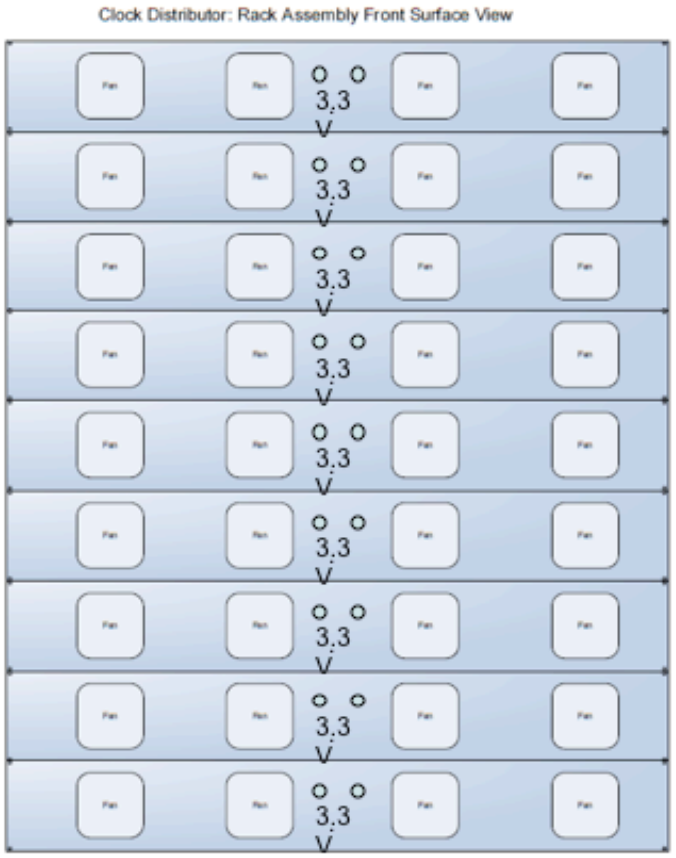


FIGURE 1B - SYSTEM OVERVIEW - CLOCK DIAGRAM 1 OF 8

Clock Distributor - Rear View



Clock Distributor - Front View



Clock Receiver

- **Sampling Functions**
  - convert light to corresponding 655.36 MHz electrical signal
  - clean up the short-term jitter of the clock using a stable PLL
  - divide the clock by 4 for 163.84 MHz clock for synchronous A/D logic
- **Tick Functions**
  - Divide the sampling clock by 655360000 to generate a SCTN (1 pps)
  - demodulate the broadcast 1 pps
  - reset SCTN when armed and 1pps is received

Clock Receiver (cont'd.)

- **Monitor & Control Functions**
  - talks to receiver's SBC through the I2C bus interface
  - monitor: voltages, laser signal detect, PLL lock state, difference between local SCTN and distributed 1 PPS
  - control: arm SCTN resync on next received 1 PPS
- **Implementation**
  - Clock receiver PCB within next generation receiver
  - High quality PLL maintains local timing, with steering from distributed GPS

Clock Subsystem - Test Plan

- Measurement of rms phase jitter between two independent clock receivers
- Most demanding spec is 10 ps rms over 10 ms sampling time
- Environmental testing - temperature cycling for boards and fibre
- M&C testing

Development Schedule