



MWA Correlator Status

Cambridge MWA Meeting

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Correlator Requirements

- Complex cross-multiply and accumulate data from 524800 signal pairs
- Each pair comprises 3072 channels with 10 KHz bandwidth
- 10 KHz bandwidth \rightarrow 30 Km wavelength, thus array is $\lambda / 20$ within a channel, **regardless of direction!**
- Max fringe-rate of 0.109 Hz for 1.5 km baseline at 300 MHz would allow dump rate of 2 s (which is v.1 int. period); 0.5 s used for solar & transients, longer baselines, minimize coherence loss
- **No fringe rotation or delay compensation necessary in hardware!**

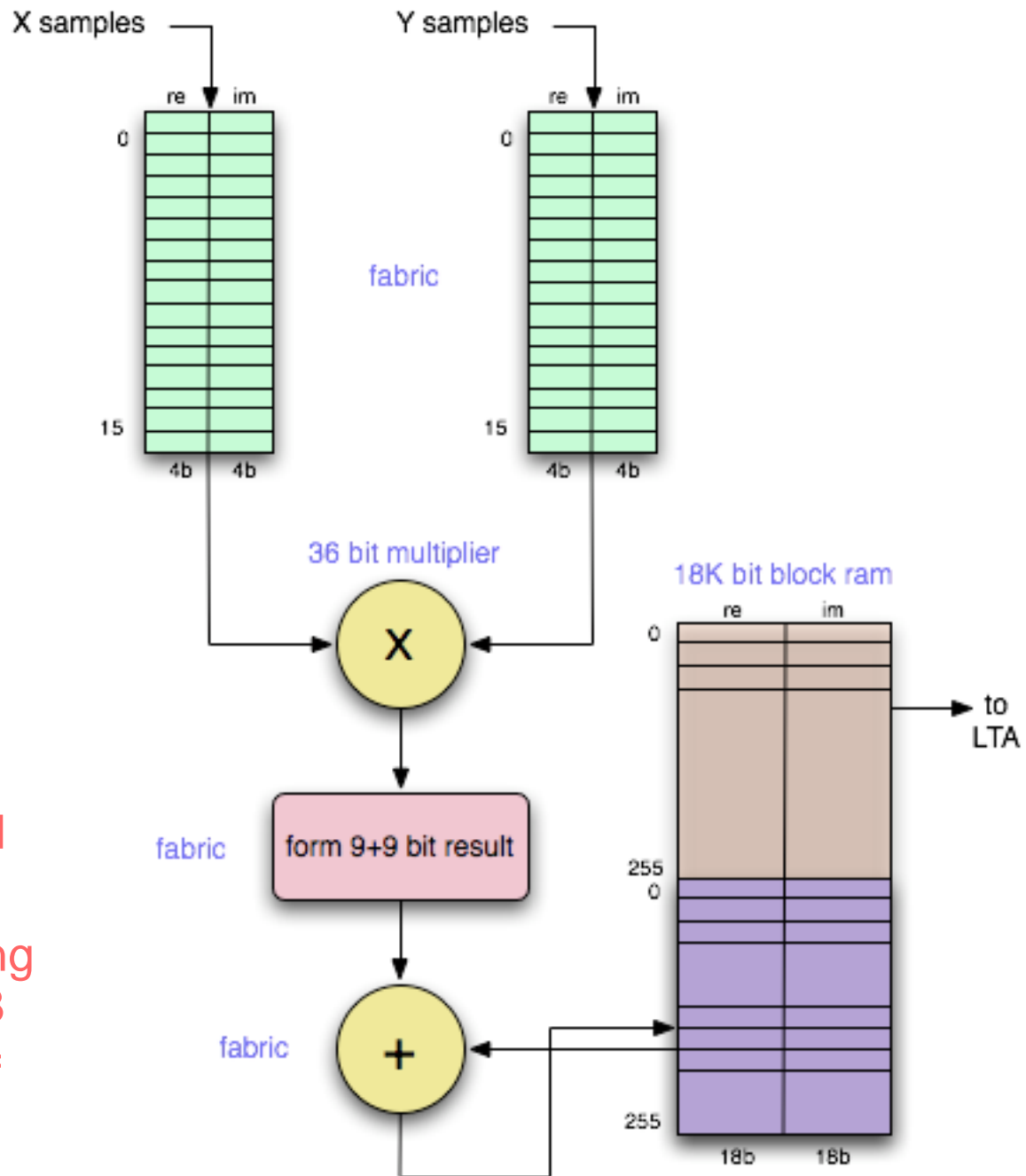


Numerology

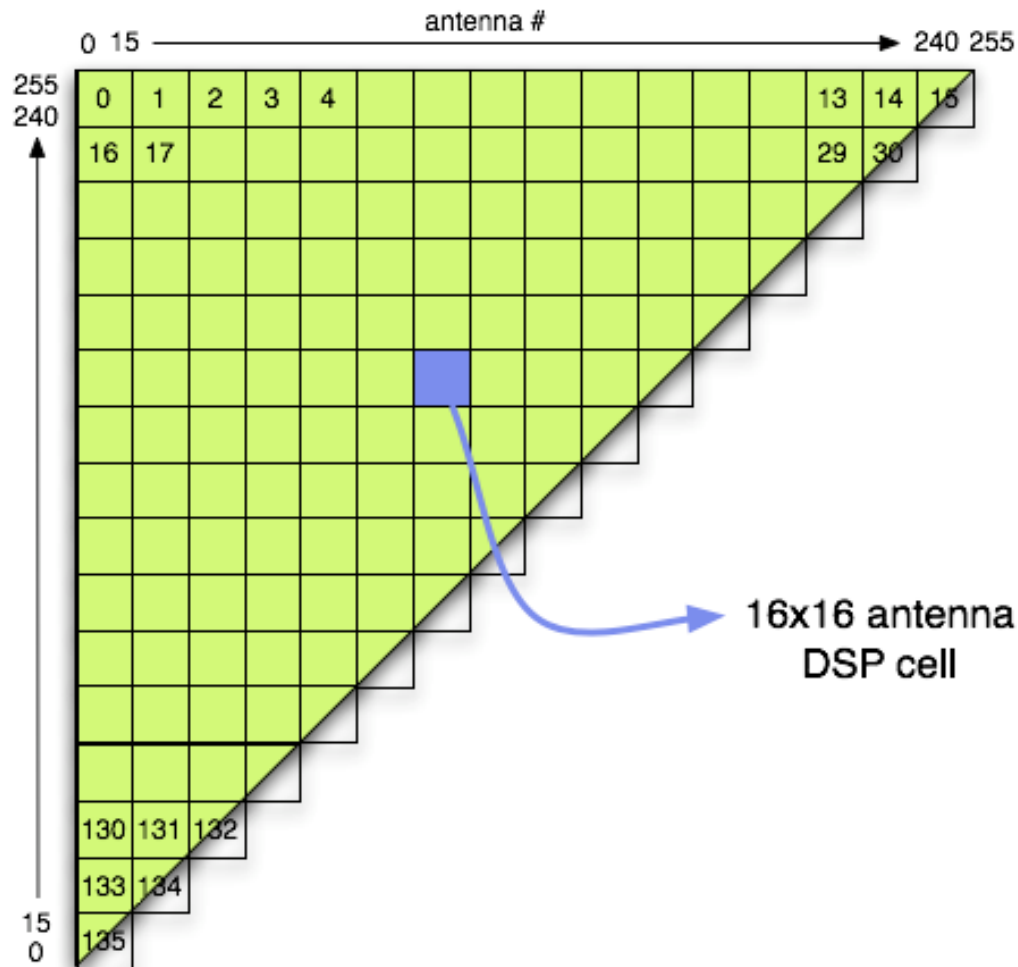
- 1 correlator board has 8 SX-35's, each with 136 cells, which can process a total of 278528 signal pairs
- Each pair of correlator boards processes 96 channels (0.967 MHz)
- 32 board pairs required for all 3072 channels (30.94 MHz)
- Requires six 19" AdvancedTCA shelves

Correlator cell

- 16 X & 16 Y 8 bit input values in distributed RAM, for a single point in time
- complex 4+4 bit multiply encoded into single 36 bit hardware multiply
- 18 bit adder implemented in local fabric
- short-term sums ping pong in block RAM: 2 comp x 18 bit x 256 prod x 2 buffers = 18 Kb

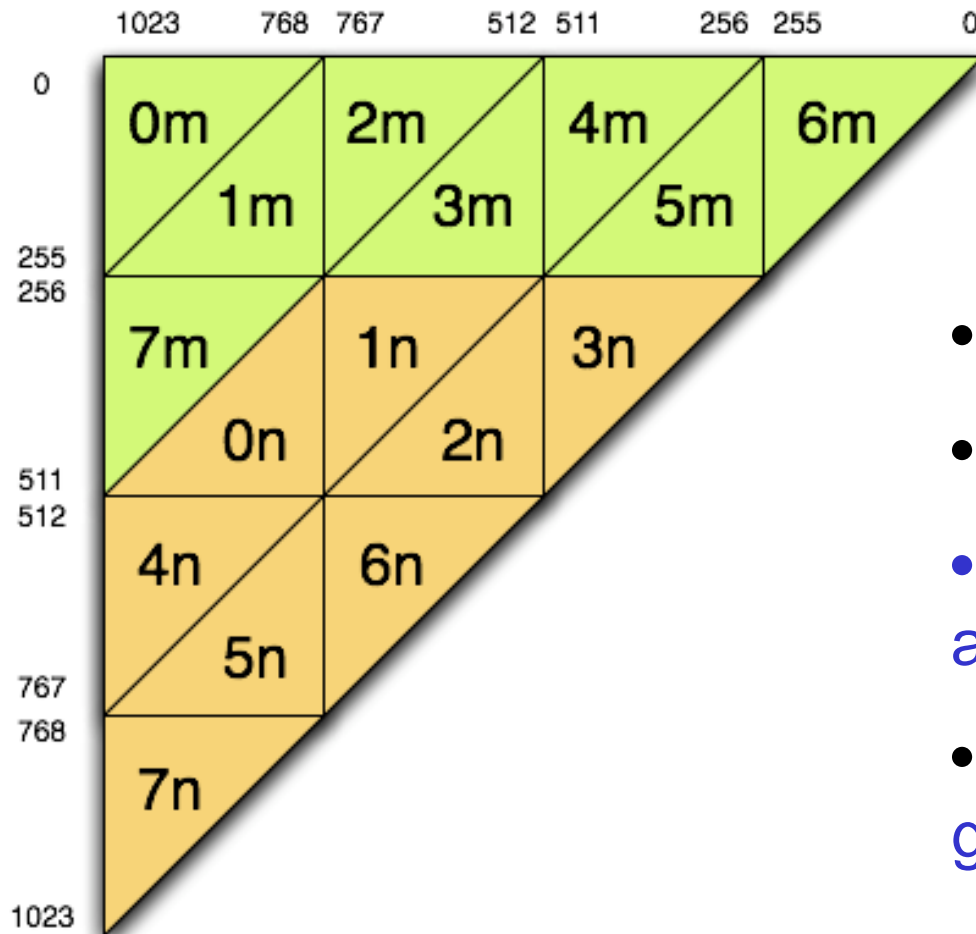


Cells mapped onto SX-35 chip



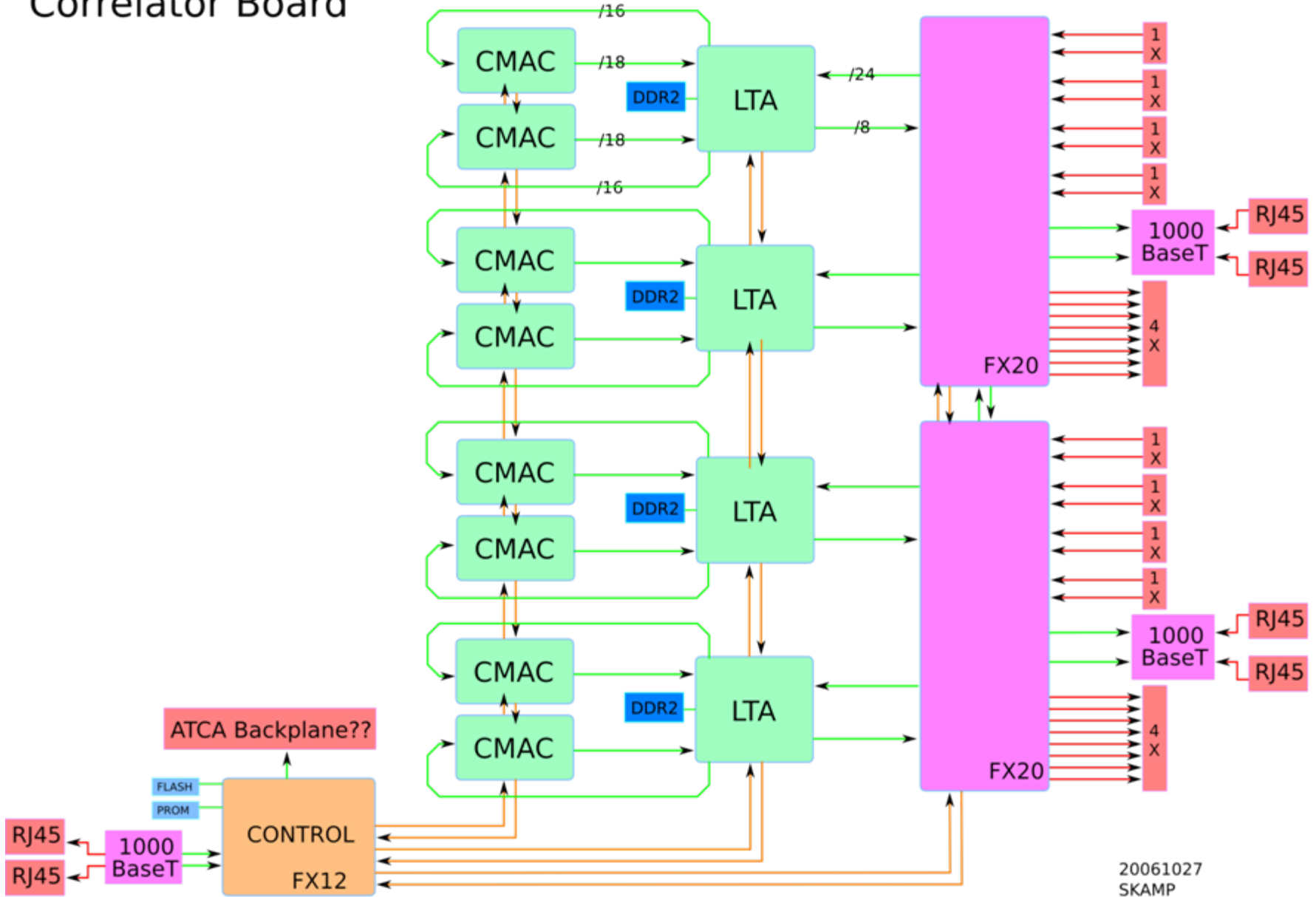
- Separate groups of 256 antennas to X and to Y
- Uses 136 of 192 available DSP slices

Two boards cover all baselines



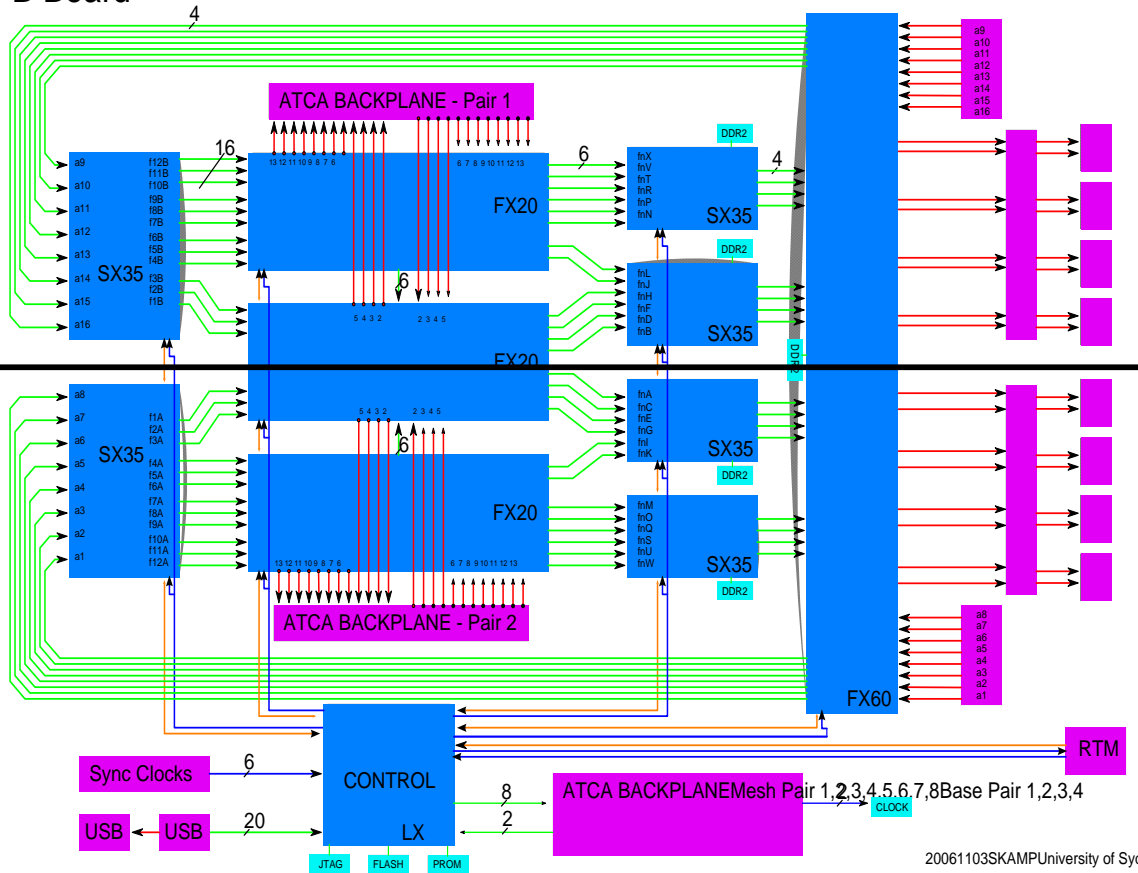
- 2 boards: m and n
- CMAC chips 0..7
- axis of symmetry along hypotenuse
- reverse input order to get lower diagonal half

Correlator Board



PFB board

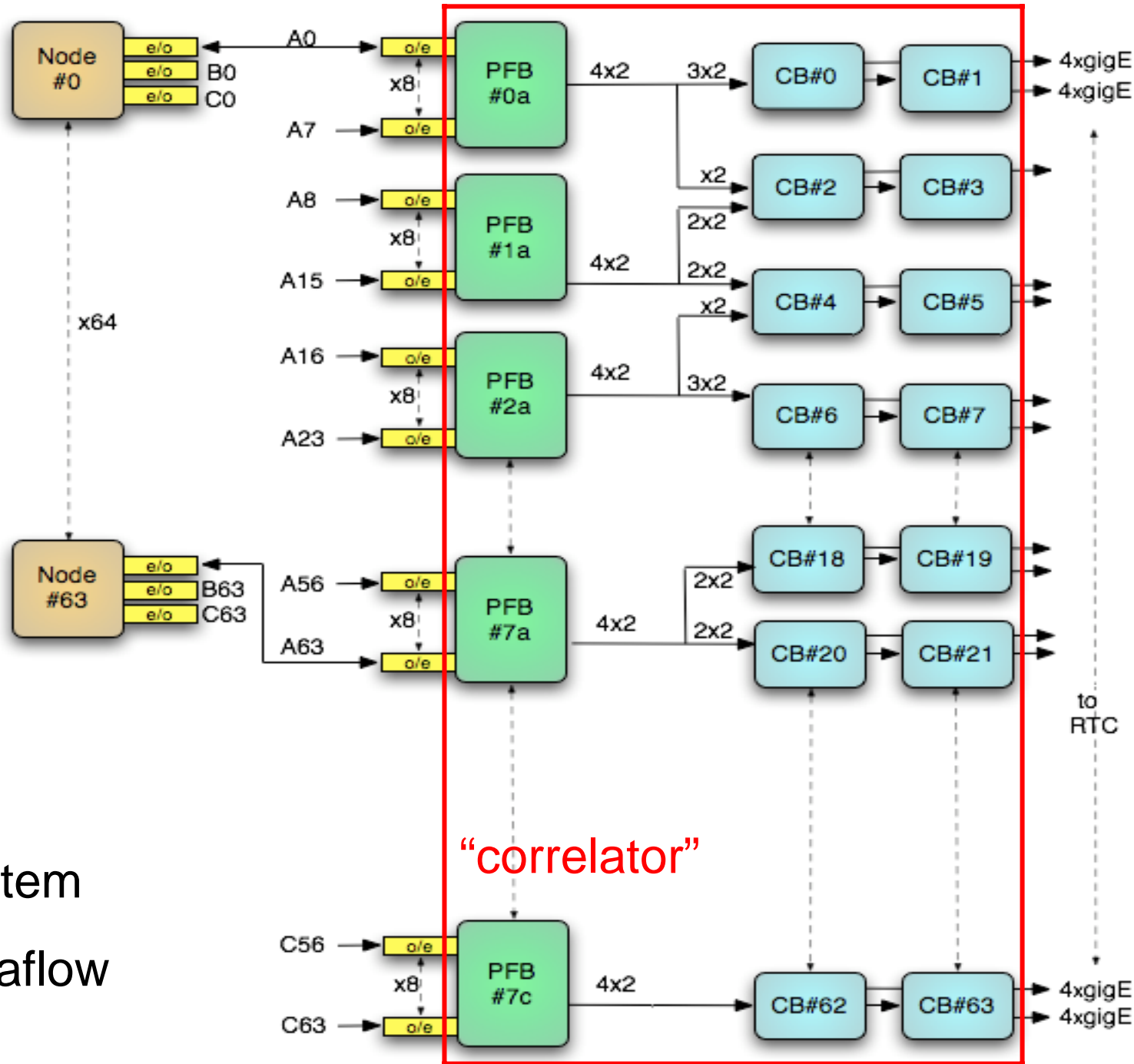
PFB Board



- Developed by SKAMP project
- Reorganizes data by coarse channel
- Breaks each 1.3 MHz coarse channel into 128 10KHz channels
- Permutes data order for correlator

Diagram Ludi deSouza

20061103SKAMP University of Sydney / CSIRO



System
Dataflow

“correlator”



Array Beamformer

- For each frequency channel, need to form a linear combination of all 1024 antennas:

$$V = \sum a_n \times g_n$$

- 16 dual polarization beams are formed (but treated internally as 32 single polarization beams)
- Computational load ~1.0 TCMAC/s
 - only 6% of correlator load of 16.2 TCMAC/s
 - possibly will be done in routing chips (FX-40's)

ABF not needed for 32T system, so detailed development has not yet begun



ABF Gains

If every beam, baseline, and channel gain were independently specified, it would require 1 TB/s of coefficient data! But...

- Complex gains g_n are a product of
 - instrumental gain - slow t variation, $g_i(\theta, \phi)$
 - ionospheric phase - medium t variation, $g_s(\theta, \phi)$, f^{-2} freq dependence
 - geometric phase - rapid f variation (linear), $g_g(\theta, \phi)$
- Time and frequency sampling can be somewhat coarse (TBD)
- Gain coefficients will be formed in RTC, in distributed fashion, and sent to the correlator FX-40's through the gigE return path



SKAMP/MWA Polyphase Filterbank Board Status

- Development funded through University of Sydney
- Schematic design and layout completed June 2007
- Routing currently being done at RRI in Bangalore, with fabrication to follow
- Prototype delivery in 2007Q3
- Firmware in development at ATNF by Ludi de Souza
 - Memory interface and PFB complete
 - Still to be done: data routing and data reordering
- Check-out and debug will take ~3 months

SKAMP/MWA

Correlator Board Status

- Development funded through University of Sydney
- Finishing touches being put on schematic design
- Layout will likely be done by RRI
- Prototype delivery in 2007Q3
- Firmware under development at Haystack
 - 136 cell version of CMAC works at ~200 MHz
 - 40 cell version (for 32T) works at full speed
 - Ethernet core designed into control chip
 - Only data routing from control to CMAC remains
- Check-out and debug with board **expected** to take ~2 months



Correlator RTM Status

- Same board works for both SKAMP and MWA
- Schematic nearly complete
- Preliminary parts placement (2 options)



PFB RTM Status

- Different for SKAMP and MWA
 - Fiber optic inputs from node different
 - Infiniband connectors to CB same
- John Russell & co. will probably do both designs (possibly with additional funding from MWA)
- SKAMP version has completed schematics and placement

Other boards & rack status

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- Slot1 controller schematics & placement complete, on hold until CB design finalized
- Slot1 RTM only at preliminary schematic stage
- Front panel boards (generic - LED's, buttons) TBD
- Full mesh backplanes, ATCA shelves are OTS items; not yet ordered





Xilinx FPGA Acquisition Plan

- 1839 total Xilinx chips in receiver and correlator
- Retail cost estimated to be \$980K
- Hoped that the chips will be provided gratis or at a deep discount via the Xilinx University Program
- For 32T, only need 66 chips for \$41K
- Real need will come in 2008 during 512 tile buildout
- SKAMP also interested in acquiring a significant number; coordination under consideration (raises numbers to 2556 chips for \$1.28M)